Silicone substrate with *in situ* strain relief for stretchable thin-film transistors

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We have manufactured stretchable thin-film transistors and interconnects directly onto an engineered silicone matrix with localized and graded mechanical compliance. The fabrication only involves planar and standard processing. Brittle active device materials are patterned on non deformable elastomer regions (strain <1% at all times) while interconnects run smoothly from "stiff" to "soft" elastomer. Pentacene thin-film transistors sustain applied strain up to 13% without electrical degradation and mechanical fracture. This integrated approach opens promising options for the manufacture of physically adaptable and transformable circuitry. © *2011 American Institute of Physics*. [doi:10.1063/1.3570661]

Electronic device materials are brittle. They fracture at extremely low strain, typically tenths of a percent.[1] Their integration onto inherently elastic substrates such as a silicone elastomer and use for stretchable electronics therefore require a careful mechanical design. Two following mechanical conditions must be fulfilled to produce elastic circuitry: (i) the strain within the transistor or circuit stack must remain below the materials' fracture strain i.e., ≪1%, during fabrication and use, and (ii) the strain profile along the interconnects running from the stiff materials to the soft matrix should be as monotonous as possible. Here we show that it is possible to engineer the elastic substrate with built-in strain relief, i.e., a polymeric matrix with graded and localized mechanical compliance, and integrate it with the fabrication of robust thin-film transistors (TFTs) and thin metal film interconnects. The strain within the TFT stack is ~0.1% when the substrate is stretched by 10%. The stretchable pentacene TFTs operate in the (−60)–(0) V range, and show a maximum current of 1 μA, a saturation mobility of 0.1 cm^2/V s, a threshold voltage of ~−5 V and an on/off ratio of ~10^4, independently of the applied uniaxial stretch.

Non deformable thin-film platforms can be produced on uniform polydimethylsiloxane (PDMS), when their stiffness is much larger than that of the substrate ($E_{platform} \times t_{platform} \gg E_{PDMS} \times t_{PDMS}$ with t the thickness and E the equivalent elastic modulus) and the platforms' lateral length is much smaller than the PDMS thickness, which is usually 0.1–1 mm.[2] A TFT stack is typically 0.5−1 μm thick and made of materials with elastic moduli in the range of tens of gigapascal.[3] Because the fabrication of TFTs on PDMS mainly relies on patterning using foil-based shadow masks, their footprint is large, e.g., a few square millimeter. The TFT stacks are not stiff enough to prevent expansion beyond fracture when the underlying PDMS substrate is stretched; the TFTs fail mechanically then electrically.[4,5]

To accommodate non uniform strain profiles along the stretchable interconnects and peak strain concentration at the hard-to-soft interface, wavy and bridge designs are often adopted to provide strain relief within the interconnects.[6–8] In turns, these imply a complex process flow and preferential stretch directions.

Here, we propose to use an engineered polymeric membrane with photopatternable (PP) mechanical compliance as a substrate. PP-PDMS is prepared by mixing a photoinhibitor solution to standard PDMS.[9] Subsequent UV exposure impedes cross-linking thus produces locally softer elastomer. To further strengthen the elastomer, polyimide islands (PIs) may be distributed and embedded at the bottom of the elastomer membrane. The TFTs are then patterned onto the stiffest regions of the elastomer; their interconnects run across the mechanically graded elastomer. Processing all device materials on the top surface of the elastomer prevent issues associated with steep and sharp step coverage of the interconnects when the devices are patterned directly on the PI island. Figures 1(a) and 1(b) present a schematic view and a top-view image of a stretchable pentacene TFT manufactured
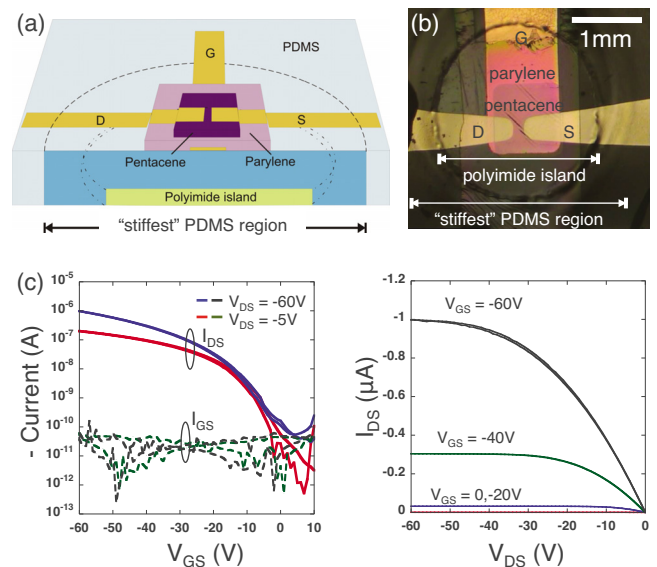

FIG. 1. (Color online) Schematic (a) and optical (b) views of a single pentacene TFT on engineered substrate. The 2.88 MPa stiff PP-PDMS region is surrounded by 1.35 MPa soft PP-PDMS. (c) Transfer (left) and output (right) characteristics of a W/L=1.33 pentacene TFT on engineered substrate.

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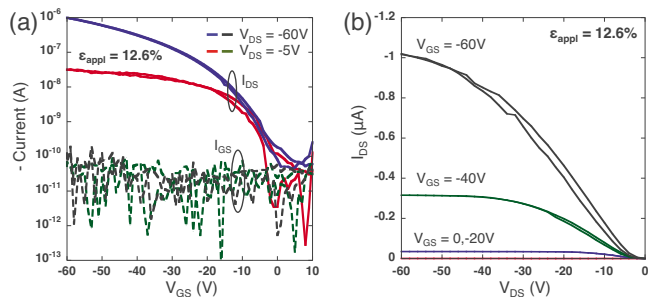
FIG. 2. (Color online) Transfer (left) and output (right) characteristics of a W/L=1.33 pentacene TFT on engineered substrate held stretched at 12.7% strain.

on such substrate. The fabrication process starts with the definition of PI islands (2 mm in diameter, 50 μm thick, 6 mm apart) on a silicon wafer coated with a water-soluble release layer. The wafer is then coated with a ~100 μm thick PP-PDMS layer. PP-PDMS preparation is described in details in Ref. 9. PP-PDMS is UV-exposed through a positive mask (UV dose=1.2 J cm^{-2}) to define "stiff" 2.4 mm diameter regions concentric with the PI islands. The equivalent elastic moduli (based on the Money–Rivlin model of the elastomer) of the non exposed and UV irradiated PP-PDMS are 2.88 MPa and 1.35 MPa, respectively.[9] The engineered polymeric membrane is then cured for 24 h at 150 °C in an air oven. To simplify the final peeling process, the graded substrate is mounted on a plastic foil (Kapton HN, Dupont) and the bottom gate staggered organic TFT process begins. The TFT stack consists of a thermally evaporated, 5 nm/30 nm thick chromium/gold (Cr/Au) bilayer (gate electrode), a 600 nm thick poly-para-xylylene (parylene C, Labcoater 2010, Specialty Coating Systems) dielectric layer, and a thermally evaporated 50 nm thick pentacene film (98% purity, Sigma, Aldrich). A 30 nm thick gold film for the source and drain contacts completes the TFTs. Each thin film is patterned using a shadow mask and aligned by eye.

The electromechanical characterization of the devices is conducted in a N_2 environment glovebox fitted with a manual stretcher. The TFTs (W/L=200 μm/100 μm) on engineered substrate are peeled off their Kapton backing (bending radius ~2 mm) then mounted free-standing in the stretcher. The device films are crack-free [Fig. 1(b)], which is a key condition for their electrical functionality. Standard probes contact the gold pads on PDMS via a compliant silver polymer dag (ESL1901-s, Electroscience Laboratories). The transfer and output characteristics of a pentacene TFT on engineered substrate are presented in Fig. 1(c). No strain is applied to the device. The TFT operates in the (−60)–(0) V range. The saturation mobility μ_{sat} is 0.105 cm^2/V s, the on-off ratio is 8.6×10^3, and the threshold voltage V_t is −5 V. The device has a low leakage gate current of 6×10^{-11} A. This performance is comparable to that reported from pentacene TFTs on PDMS (Ref. 5) and flexible substrates.[10]

Figure 2 summarizes the I(V) curves of the pentacene TFT held at 12.6% strain. The TFT response is little affected by the large mechanical deformation with μ_{sat} =0.106 cm^2/V s and V_t=−4 V. The small hysteresis observed in the output curves is attributed to the electrical contact between the polymer Ag dag and the tungsten probes, which need to be lifted up and repositioned at each strain.
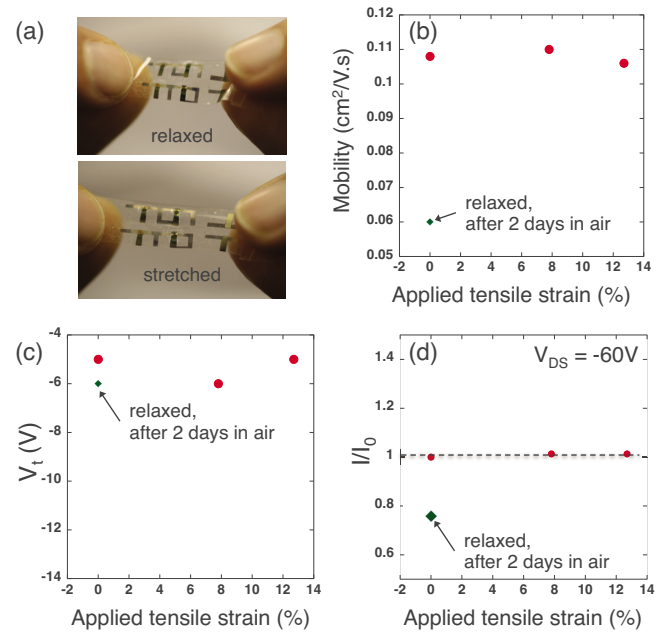

FIG. 3. (Color online) (a) Optical views of stretchable TFTs on engineered substrate. (b) Saturation mobility, threshold voltage and channel on current as a function of applied mechanical strain.

Figure 3(a) illustrates a membrane with six TFTs uniaxially stretched. The longitudinal extension of the Au interconnects in-between the TFTs is clearly visible. Figures 3(b)–3(d) summarizes the TFT response with strain. Negligible changes in mobility, V_t and output current of the device are observed. Stretching further (>13%) often results in delamination of the polymer Ag dag from the soft substrate. After release, the TFTs are not probed but kept for two days in air. Under the optical microscope, the device films appear smooth and crack-free after the mechanical stretching cycle indicating that the strain within the TFT stack did not exceed their fracture strain. After two days in air, the TFTs remain functional but their electrical performance has degraded. This is attributed to the oxidation of the pentacene rather than mechanical damage to the TFT channels.

To quantify the strain levels and distribution within the engineered substrate, we simulate the deformation of the substrate under 10% tensile applied strain using three-dimensional finite element modeling (Comsol). The elastomer is simulated with the hyperelastic Mooney–Rivlin model and fitted parameters from experimental stress-strain curves.[9,11] The 730 nm thick TFT stack is not modeled. The engineered substrate is 100 μm thick; the PI island is 50 μm thick, 2 mm diameter. Figures 4(a) and 4(b) show two strain color plots of the substrate with a PI island embedded in a uniform and 2-moduli PP-PDMS, and strain profiles at the top surface of the engineered substrates, ε_{top}. A uniform PDMS substrate expands uniformly, the strain across the whole substrate equals the applied strain (data not shown). When a PI island is embedded at the bottom of a uniform PDMS substrate, ε_{top} is pinned to 0.1% in the region immediately above the PI island then increases to $\varepsilon_{top,max}$ ~18.1%, a few hundreds of micrometer beyond the island edge (profile A-A, Fig. 4) and decreases to 10% strain away from the island. The diameter of the ~0% region aligned with the PI island is 1.1mm. Using a 2-moduli PP-PDMS with its stiffest region centered on the PI island allows for
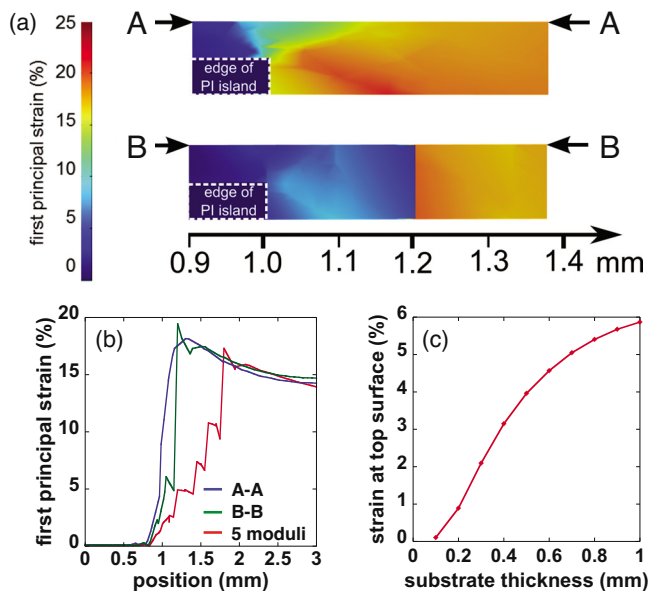
FIG. 4. (Color online) Finite element modeling of engineered substrates with built-in strain relief. (a) First principal strain color cross-sections of substrates prepared with (top) a uniform PP-PDMS membrane (1.35 MPa), and (bottom) a 2-moduli PP-PDMS membrane (2.88 MPa; 2.4 mm diameter and 1.35 MPa matrix). The *x*-axis runs along the radius of the 50 μm thick PI island and starts at its center (x=0). (b) Strain profiles at the top surface of the elastomer for three types of substrates: Uniform, 2-moduli, and 5 moduli PP-PDMS membranes. The 5-moduli substrate is designed with concentric PP-PDMS rings of 2.88 MPa; 2.4 mm diameter, 1.8 MPa; 2.8 mm diameter, 1.35 MPa; 3.2 mm diameter, 0.96 MPa; 3.6 mm diameter, and 0.65 MPa for the matrix. (c) Strain at the center of the stiff elastomer surface (x=0) as a function of the thickness of the PP-PDMS membrane.

the widening of the no-deformation region at the top surface (profile B-B, Fig. 4). Using a 2.4 mm diameter, 2.88 MPa stiff PP-PDMS volume surrounded by 1.35 MPa soft PP-PDMS allows for a 1.6 mm diameter undeformable region above the PI island. Note that the striking color transition at x=1.2 mm comes from the discrete boundaries between the two elastomers of different modulus. Further simulations show that using more steps in the compliance gradient [a 5-moduli elastomer is used Fig. 4(b)] further widens the ~0% region at the surface of the elastomer (to 1.7 mm diameter) but more importantly the strain increase across the stiff-to-soft interface may be greatly reduced (from 48%/mm with no grading down to 15%/mm with 5-moduli). This could be achieved by exposing the PP-PDMS membrane with five successive UV exposures through five concentric positive masks or in a single exposure using a graded binary mask (experiments not done). Finally the pinning to nearly

0% strain of the top elastomer surface depends on the PI island to elastomer thickness ratio, R. Figure 4(c) plots ε_{top} at x=0 mm i.e., above the center of the PI island, as a function of the elastomer thickness for a 50 μm thick PI island. The applied strain is 10%. ε_{top} increases quickly to values above 1% when the substrate is thicker than 200 μm. This suggests R should be at least 0.25.

In summary, we have demonstrated that stretchable thin-film transistors can be fabricated directly onto elastomeric substrates. The proposed strain relief method based on photopatterned graded stiffness of the elastomer combined with embedded plastic islands is efficient to ensure TFT materials are not stretched above their fracture strains ($<$1%), and can be tuned to develop a low strain profile across the elastic thin film interconnects running in-between the nondeformable elastomeric regions. Furthermore this method is not limited to organic TFTs and should be easily transferred to other thin-film devices including low temperature amorphous silicon and zinc oxide TFTs. The direct integration of microelectronic devices onto engineered elastomeric substrates has the potential to influence the design of most existing stretchable circuits and therefore, opens up a wide range of exciting opportunities.

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